42V$_{IN}$, 0.5A, Asynchronous Step-Down Converter with Low Quiescent Current

General Description

The RT6340 is a 0.5A, high-efficiency, peak current mode control asynchronous step-down converter. The device operates with input voltages from 4V to 42V. The device can program the output voltage between 0.8V to VIN. The low quiescent current design with the integrated low $R_{DS(ON)}$ of high-side MOSFET achieves high efficiency over the wide load range. The peak current mode control with simple external compensation allows the use of small inductors and results in fast transient response and good loop stability.

The wide switching frequency of 100kHz to 2500kHz allows for efficiency and size optimization when selecting the output filter components. The ultra-low minimum on-time enables constant-frequency operation even at very high step-down ratios. For switching noise sensitive applications, it can be externally synchronized from 300kHz to 2200kHz.

The RT6340 provides complete protection functions such as input under-voltage lockout, output under-voltage protection, output over-voltage protection, over-current protection, and thermal shutdown. Cycle-by-cycle current limit provides protection against shorted outputs, and soft-start eliminates input current surge during start-up. The RT6340 is available in WDFN-10SL 3x3 and SOP-8 (Exposed pad) packages.

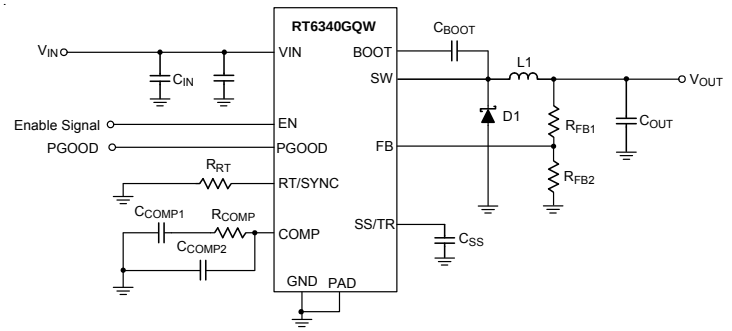
Features

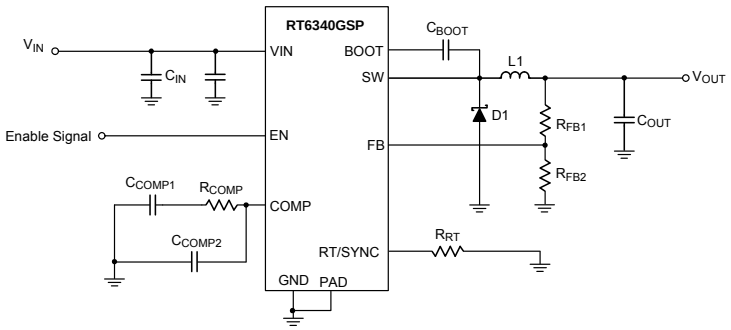
- **Wide Input Voltage Range**
  - **4.5V to 42V**
  - **4V to 42V (Soft-start is finished)**
- **Wide Output Voltage Range : 0.8V to VIN**
- **0.8V ±1.5% Reference Accuracy**
- **Peak Current Mode Control**
- **Integrated 170mΩ High-Side MOSFET**
- **Low Quiescent Current : 90μA**
- **Low Shutdown Current : 1.3μA**
- **Adjustable Switching : 100kHz to 2.5MHz**
- **Synchronizable Switching : 300kHz to 2.2MHz**
- **Power Saving Mode (PSM) at Light Load**
- **Low Dropout at Light Loads with Integrated Boot Recharge FET**
- **Externally Adjustable Soft-Start by Part Number Option**
- **Power Good Indication by Part Number Option**
- **Enable Control**
- **Adjustable UVLO Voltage and Hysteresis**
- **Built-In UVLO, UVP, OVP, OCP, OTP**

Applications

- 12V and 24V Power Systems
- GPS, Entertainment

Simplified Application Circuit





Ordering Information

RT6340 □□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
  (WDFN-10SL 3x3 only)
- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
  QW : WDFN-10SL 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

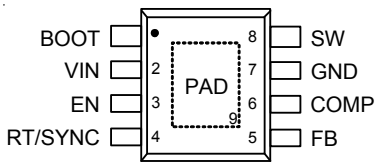
***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

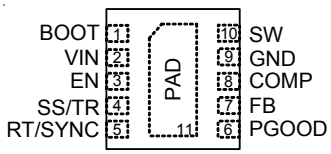
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



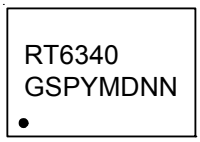
SOP-8 (Exposed pad)



WDFN-10SL 3x3

Marking Information

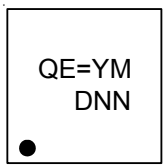
RT6340GSP



RT6340GSP : Product Number

YMDNN : Date Code

RT6340GQW



QE= : Product Code

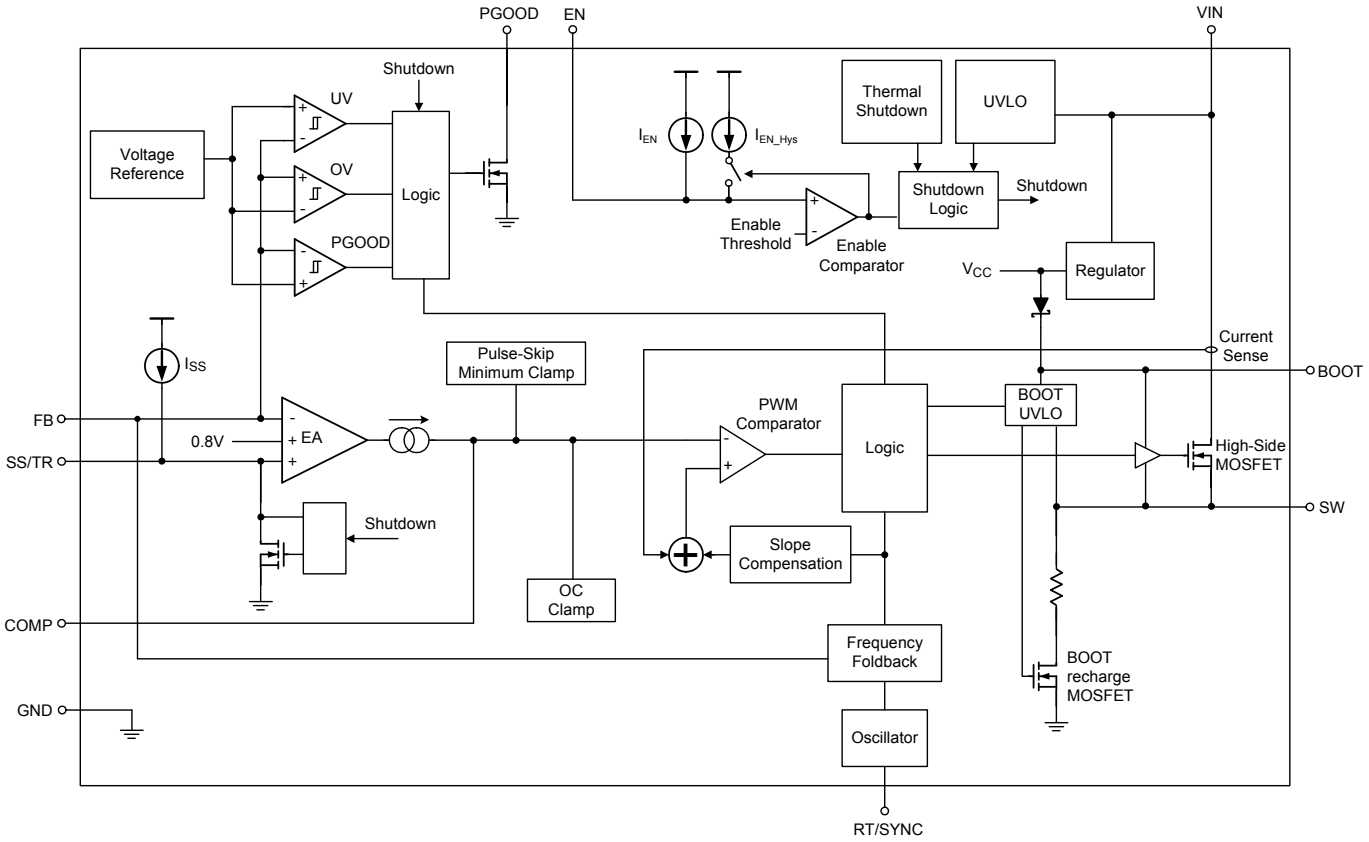
YMDNN : Date Code

Functional Pin Description

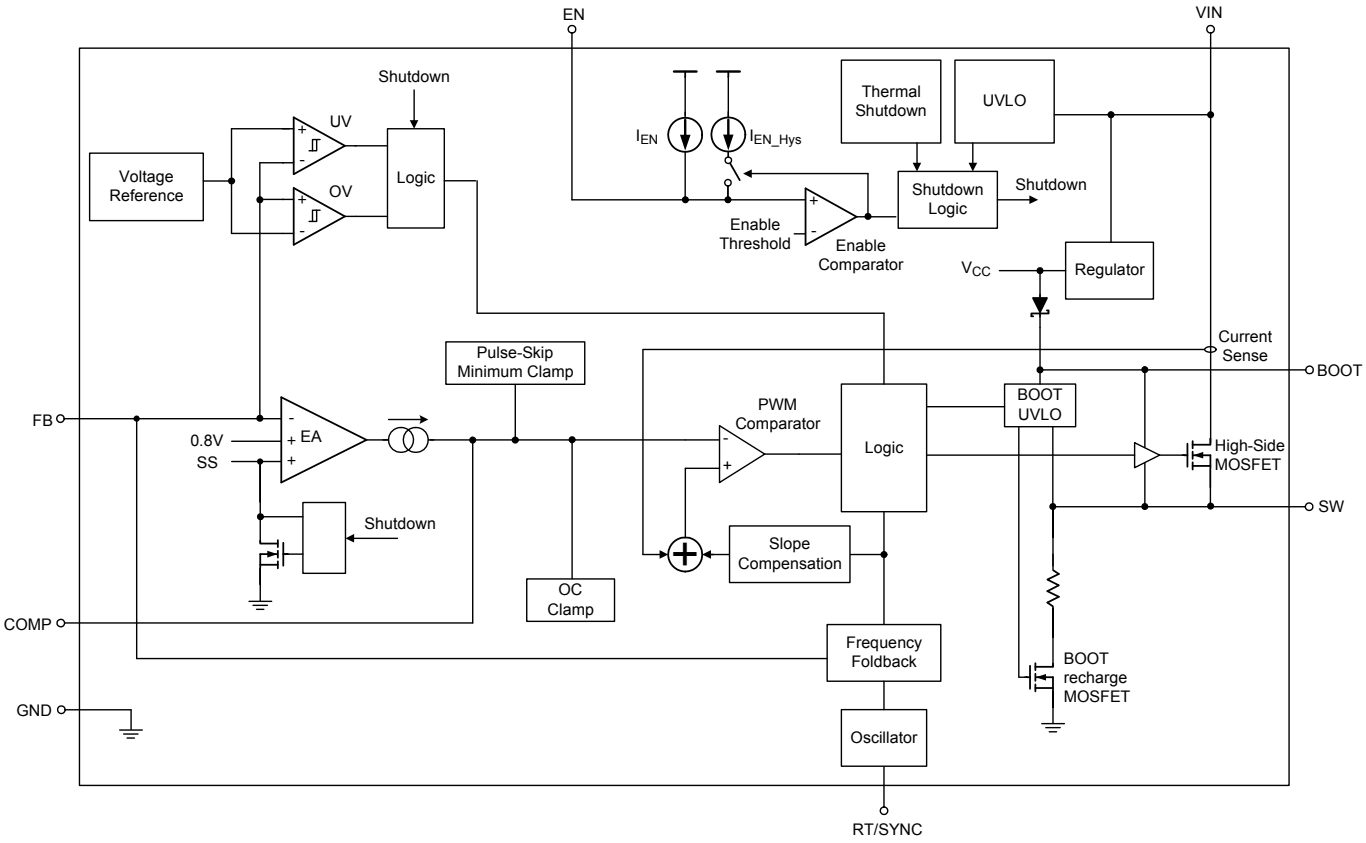
Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10SL 3x3		
1	1	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the SW pin.
2	2	VIN	Power input. The input voltage range is from 4V to 42V. Connect a suitable input capacitor between this pin and GND, usually two 2.2μF or larger ceramic capacitors with one typical capacitance 4.7μF.
3	3	EN	Enable control pin with internal pull-up current source. Float or provide a logic-high (≥ 1.25V) enables the converter; a logic-low forces the device into shutdown mode.
--	4	SS/TR	Soft-start and tracking control input. Connect a capacitor from SS to GND to set the soft-start period. "Do Not" leave this pin floating to avoid inrush current during power up. It also can be used to track and sequence because the SS/TR pin voltage can override the internal reference voltage.
4	5	RT/SYNC	Frequency setting and external synchronous signal input. Connect a resistor from this pin to GND to set the switching frequency. Tie to a clock source for synchronization to an external frequency.
--	6	PGOOD	Open-drain power-good indication output. Once being started-up, PGOOD will be pulled low to GND if any internal protection is triggered.
5	7	FB	Output voltage sense. Sense the output voltage at the FB pin through a resistive divider. The feedback reference voltage is 0.8V typically.
6	8	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
7	9	GND	Ground. Provide the ground return path for the control circuitry.
8	10	SW	Switch node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
9 (Exposed Pad)	11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram

WDFN-10SL 3x3 package



SOP-8 (Exposed pad) package



Operation

Control Loop

The RT6340 is a high efficiency asynchronous step-down converter utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET. At the beginning of each clock cycle, the internal high-side MOSFET turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (V_{REF}) to generate a compensation signal (V_{COMP}) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET is turned off and inductor current ramps down. While the high-side MOSFET is off, the inductor current is supplied through the external low-side diode, freewheel diode, connected between the SW pin and GND. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Light Load Operation

The RT6340 operates in power saving mode (PSM) at light load to improve light load efficiency. IC starts to switch when V_{FB} is lower than PSM threshold (V_{REF} x 1.005, typically) and stops switching when V_{FB} is high enough.

During PSM, IC controls the minimum inductor peak current (I_{L_PEAK}) by clamping the COMP level. During non-switching period, most of the internal circuit is shut down, and the supply current drops to quiescent current (90μA, typically) to reduce the quiescent power consumption. With lower output loading, the non-switching period is longer, so the effective switching frequency becomes lower to reduce the switching loss and switch driving loss.

Switching Frequency Selection and Synchronization

The RT6340 provides an RT/SYNC pin for switching frequency selection. The switching frequency can be set by using external resistor $R_{RT/SYNC}$ and the switching frequency range is from 100kHz to 2.5MHz. The RT6340 can also be synchronized with an external clock ranging from 300kHz to 2.2MHz by RT/SYNC pin. The switching frequency of synchronization should be equal to or higher than the frequency set by the RT resistor. For example, if the switching frequency of synchronization is 500kHz or higher, the $R_{RT/SYNC}$ should be selected for 500kHz.

The RT6340 implements a frequency foldback function to protect the device at over-load or short-circuited condition, especially higher switching frequencies and input voltages. The switching frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V for switching frequency control by RT resistor setting mode and the synchronization mode both. The frequency foldback function increases the switching cycle period and provides more time for the inductor current to ramp down.

Maximum Duty Cycle Operation

The RT6340 is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than minimum off-time, the RT6340 starts to enable skip off-time function and keeps high-side MOSFET on continuously.

The RT6340 implements skip off-time function to achieve high duty approaching 100% and the maximum output voltage is near the minimum input supply voltage of the application for input voltage momentarily falls down to the normal output voltage requirement. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

For normal operation, the minimum input voltage can be calculated from below equation :

$$V_{IN\_MIN} = \frac{V_{OUT} + I_{OUT\_MAX} \times R_L + V_D}{1 - f_{SW} \times t_{OFF\_MIN}} + I_{OUT\_MAX} \times R_{DS(ON)\_H} + V_D$$

where V_{IN_MIN} is the minimum normal operating input voltage; $R_{DS(ON)\_H}$ is the on-resistance of the high-side MOSFET; V_D is the forward conduction voltage of the freewheel diode; R_L is the DC resistance of inductor.

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET at any conditions. The BOOT UVLO usually actives at extremely high conversion ratio or the higher V_{OUT} application operates at very light load. With such conditions when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (2.7V, typically), the device turns on the internal BOOT recharge FET (150ns, typically) to charge the BOOT capacitor. The BOOT UVLO is sustained until the BOOT to SW voltage is higher than $V_{BOOT\_UVLO\_H}$ (2.8V, typically).

Enable Control

The RT6340 provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below the enable threshold voltage, switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLOH}). If V_{EN} is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (1.3μA, typically). If the EN voltage rises above the enable threshold voltage while the VIN voltage is higher than V_{UVLOH}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. The EN pin has an internal pull-up current source I_{EN} (0.9μA, typically) that enables operation of the RT6340 when the EN pin floats. The EN pin can be used to adjust the under-voltage lockout (UVLO) threshold and hysteresis by using two external resistors. The RT6340 implements additional hysteresis current source I_{EN_Hys} (2.9μA, typically) to adjust the UVLO. The I_{EN_Hys} is sourced out of the EN pin when V_{EN} is larger than enable threshold voltage. When the V_{EN} falls below enable threshold voltage, the I_{EN_Hys} will be stopped sourcing out of the EN pin.

Soft-Start and Tracking Control

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RT6340GSP provides internal soft-start and the RT6340GQW provides external soft-start function for inrush currents control. The RT6340GQW provides an SS/TR pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor $C_{SS/TR}$ connected from the SS/TR pin to ground or controlled by external ramp voltage to SS/TR pin. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (2μA, typically) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The high-side MOSFET will start switching if the voltage difference between SS/TR pin and FB pin is equal to 75mV (i.e. $V_{SS/TR} - V_{FB}$ = 75mV, typically) during power-up period. If the output is pre-biased to a certain voltage during start-up for some reason, the device will not start switching until the voltage difference between SS/TR pin and FB pin is equal to 75mV (typically). Only when this ramp voltage is higher than the feedback voltage V_{FB}, the switching will be resumed. The FB voltage will track the SS/TR pin ramp voltage with a SS/TR to FB offset voltage (75mV, typically) during soft-start interval. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the FB pin voltage rises above 94% of V_{REF} (typically), the PGOOD pin will be in high impedance and the V_{PGOOD} will be held high. The typical start-up waveform shown in Figure 1 indicates the sequence and timing between the output voltage and related voltage.

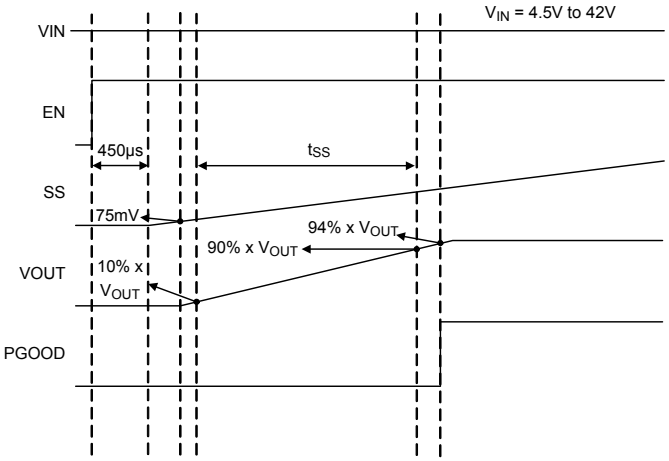


Figure 1 Start-Up Sequence for RT6340GQW

Power Good Indication

The RT6340GQW features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to an external voltage source and it is recommended to use pull-up resistance between the values of 1 and 10kΩ to reduce the switching noise coupling to PGOOD pin. The PGOOD assertion requires input voltage above 1.5V. The power-good function is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above the power-good high threshold (V_{TH_PGLH1}) (94% of the reference voltage, typically), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} falls below power-good low threshold (V_{TH_PGHL2}) (92% of the reference voltage, typically) or exceeds V_{TH_PGHL1} (109% of the reference voltage, typically), the PGOOD pin will be pulled low. For V_{FB} higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (106% of the reference voltage, typically). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device (6Ω, typically) will pull the PGOOD pin low. The power good indication profile is shown in Figure 2.

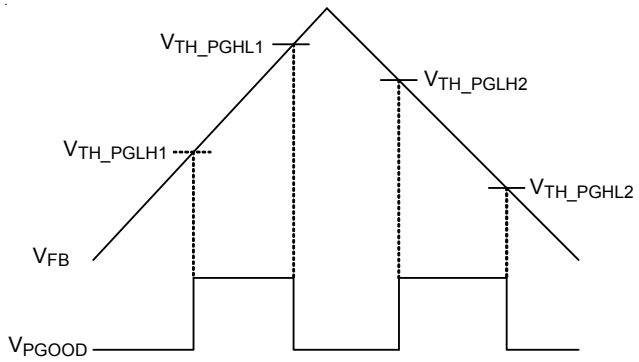


Figure 2. The Logic of PGOOD for RT6340GQW

Input Under-Voltage Lockout

In addition to the EN pin, the RT6340 also provides enable control through the VIN pin. If V_{EN} rises above V_{TH_EN} first, the switching will be inhibited until the VIN voltage rises above V_{UVLOH}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal high-side MOSFET can be prevented. After the device is powered up, if the input voltage V_{IN} goes below the UVLO falling threshold voltage (V_{UVLOL}), this switching will be inhibited; if V_{IN} rises above the UVLO rising threshold (V_{UVLOH}), the device will resume switching. Note that V_{IN} = 4V is only design for input voltage momentarily falls down to the UVLO threshold voltage requirement, and normal input voltage should be larger than the V_{UVLOH}.

High-Side MOSFET Peak Current Limit Protection

The RT6340 includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The inductor current through the high-side MOSFET will be measured after a certain amount of delay when the high-side MOSFET being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side MOSFET to prevent the inductor current exceeding the high-side MOSFET peak current limit (I_{LIM}).

Output Under-Voltage Protection

The RT6340 includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (50% of the internal reference voltage, typically), the UV comparator will go high to turn off the internal high-side switch. If the output under-voltage condition continues for a period of time, the RT6340 enters output under-voltage protection with hiccup mode and discharges the $C_{SS/TR}$ by an internal discharging current source I_{SS_DIS} (0.5μA, typically). During hiccup mode, the device remains shutdown. After the SS pin voltage is discharged to less than 54mV (typically), the RT6340 attempts to re-start up again, and the internal charging current source I_{SS} (2μA, typically) gradually increases the voltage on $C_{SS/TR}$. The high-side MOSFET will start switching when voltage

difference between SS pin and FB pin is equal to 75mV (i.e. V_{SS} – V_{FB} = 75mV, typically). If the output under-voltage condition is not removed, the high-side MOSFET stops switching when the voltage difference between SS pin and FB pin is 1.2V (i.e. V_{SS} – V_{FB} = 1.2V, typically) and then the I_{SS_DIS} discharging current source begins to discharge $C_{SS/TR}$. Upon completion of the soft-start sequence, if the output under-voltage condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the output under-voltage condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

A short-circuit protection and recovery profile is shown in Figure 3.

Since the $C_{SS/TR}$ will be discharged to 54mV when the RT6340 enters output under-voltage protection, the first discharging time (t_{SS_DIS1}) can be calculated as below :

$$t_{SS\_DIS1} = C_{SS} \times \frac{V_{SS} - 0.054}{I_{SS\_DIS}}$$

The equation below assumes that the V_{FB} will be 0 at short-circuited condition and it can be used to calculate the $C_{SS/TR}$ discharging time (t_{SS_DIS2}) and charging time (t_{SS_CH}) during hiccup mode.

$$t_{SS\_DIS2} = C_{SS} \times \frac{1.146}{I_{SS\_DIS}}$$

$$t_{SS\_CH} = C_{SS} \times \frac{1.146}{I_{SS\_CH}}$$

Figure 3. Short-Circuit Protection and Recovery

Output Over-Voltage Protection

The RT6340 includes an output over-voltage protection (OVP) circuit to limit output voltage. Since the V_{FB} is lower than the reference voltage (V_{REF}) at over-load or short-circuited condition, the COMP voltage will be high to demand maximum output current. Once the over-load or short-circuited condition is removed, the COMP voltage resumes to the normal voltage to regulate the output voltage. The output voltage leads to the possibility of an output overshoot if the load transient is faster than the COMP voltage transient response, especially for small output capacitance. If the V_{FB} goes above the 109% of the reference voltage, the high-side MOSFET will be forced off to limit the output voltage. When the V_{FB} drops lower than the 106% of the reference voltage, the high-side MOSFET will be resumed.

Over-Temperature Protection

The RT6340 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 45V
- Enable Voltage, EN ---------- –0.3V to 45V
- Switch Voltage, SW ---------- –0.6V to 45V
- SW (t ≤ 100ns) ---------- –5V to 50V
- BOOT to SW (BOOT–SW) ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 4V to 42V
- Output Voltage ---------- 0.8V to V_{IN}
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WDFN-10SL 3x3	SOP-8 (Exposed pad)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	34.1	31.8	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	77.6	74.1	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5.9	4.9	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	38.8	31.4	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.3	14.7	°C/W

Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}	After soft-start is finished	4	--	42	V
VIN Under-Voltage Lockout Threshold	V_{UVLOH}	V_{IN} rising	4.1	4.3	4.5	V
	V_{UVLOL}	V_{IN} falling	3.8	3.9	4	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	1.3	4	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.83V, not switching	--	90	130	μA
Enable Voltage						
Enable Threshold Voltage	V_{TH_EN}		1.15	1.25	1.36	V
Enable to COMP Active		V_{IN} = 12V, T_A = 25°C	--	450	--	μs
Pull-Up Current	I_{EN}	V_{TH_EN} + 50mV	--	3.8	--	μA
		V_{TH_EN} – 50mV	--	0.9	--	μA
Hysteresis Current	I_{EN_Hys}		--	2.9	--	μA
Reference Voltage						
Reference Voltage	V_{REF}		0.788	0.8	0.812	V
Internal MOSFET						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$	V_{IN} = 12V, V_{BOOT} – V_{SW} = 5V	--	170	300	mΩ
Error Amplifier						
Input Current			--	50	--	nA
Error Amplifier Trans-Conductance	gm	Normal operation –2μA < I_{COMP} < 2μA V_{COMP} = 1V	--	97	--	μA/V
		During SS, –2μA < I_{COMP} < 2μA V_{COMP} = 1V, V_{FB} = 0.4V	--	26	--	
Error Amplifier DC Gain		V_{FB} = 0.8V	--	10000	--	V/V
Error Amplifier Bandwidth			--	2700	--	kHz
Source/Sink Current		V_{COMP} = 1V, 100mV overdrive	--	±7	--	μA
COMP to Current Sense Trans-Conductance	gm_cs		--	2	--	A/V
Current Limit						
Current Limit	I_{LIM}	f_{SW} = 580kHz, V_{OUT} = 5V	0.72	0.9	1.08	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	I_{OUT} = 1A	--	100	130	ns
Timing Resistor and External Clock						
Switching Frequency 1	f_{SW1}	$R_{RT/SYNC}$ = 1.2MΩ	85	100	115	kHz
Switching Frequency 2	f_{SW2}	$R_{RT/SYNC}$ = 200kΩ	520	580	640	kHz
Switching Frequency 3	f_{SW3}	$R_{RT/SYNC}$ = 44.2kΩ	2250	2500	2750	kHz
SYNC Frequency Range		External clock	0.3	--	2.2	MHz
Minimum Sync Pulse Width			--	40	--	ns
SYNC Threshold Voltage	V_{IH_SYNC}		--	1.9	2.2	V
	V_{IL_SYNC}		0.5	0.7	--	
RT/SYNC Falling Edge to SW Rising Edge Delay			--	60	--	ns
Soft-Start and Tracking						
Internal Charge Current	I_{SS}	$V_{SS/TR}$ = 0.4V, RT6340GQW	--	2	--	μA
SS/TR to FB Offset		$V_{SS/TR}$ = 0.4V, RT6340GQW	--	75	--	mV
SS/TR-to-Reference Crossover		98% nominal, RT6340GQW	--	0.9	--	V
SS/TR Discharge Voltage		V_{FB} = 0V, RT6340GQW	--	54	--	mV
Internal Soft-Start Time						
Soft-Start Period		10% to 90%, RT6340GSP	1.4	2	2.6	ms
Power Good						
Power Good Threshold	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF}, PGOOD from low to high, RT6340GQW	90	94	98	%
	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF}, PGOOD from high to low, RT6340GQW	105	109	113	
	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF}, PGOOD from high to low, RT6340GQW	88	92	96	
	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF}, PGOOD from low to high, RT6340GQW	102	106	110	
Power Good Hysteresis		V_{FB} falling, RT6340GQW	--	2	--	%
Power Good Leakage Current	I_{LK_PGOOD}	V_{PGOOD} = 5.5V, T_A = 25°C, RT6340GQW	--	10	500	nA
On-Resistance		I_{PGOOD} = 3mA, V_{FB} < 0.79V, RT6340GQW	--	6	15	Ω
Minimum VIN for defined output		V_{PGOOOD} < 0.5V, I_{PGOOD} = 100μA, RT6340GQW	--	0.95	1.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
Thermal Shutdown	T_{SD}		--	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	°C
Output Under-Voltage Protection						
UVP Trip Threshold	V_{UVP}	UVP detect	--	0.4	--	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

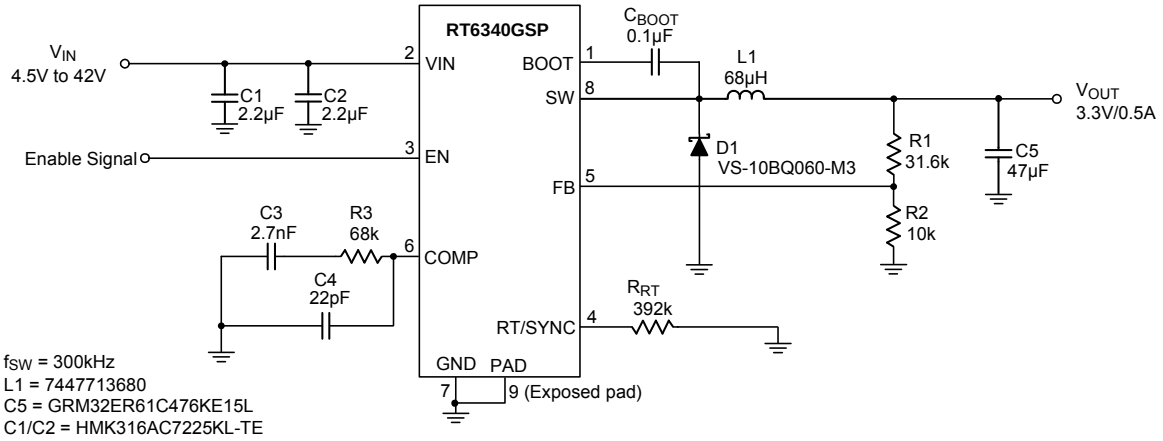
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm, furthermore, outer layers with 2 OZ. Cu and inner layers with 1 OZ. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

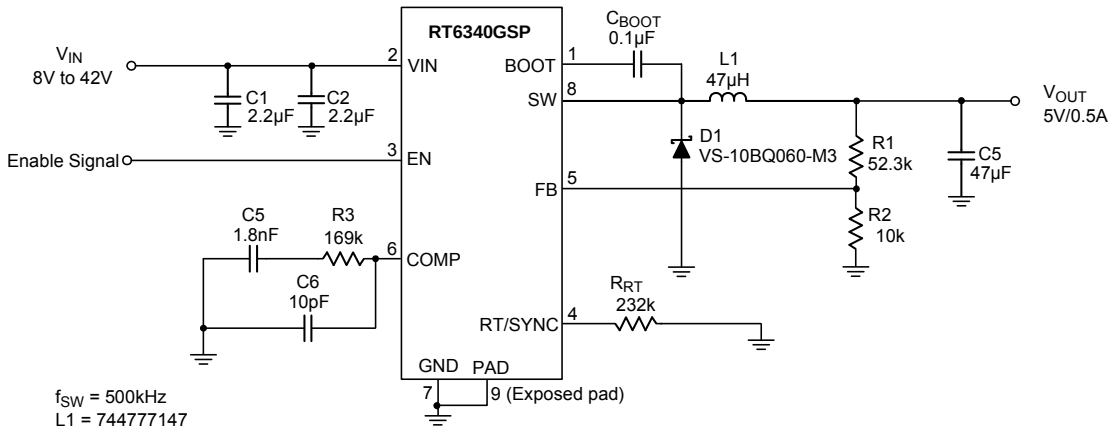
Typical Application Circuit

300kHz, 3.3V, 0.5A Step-Down Converter



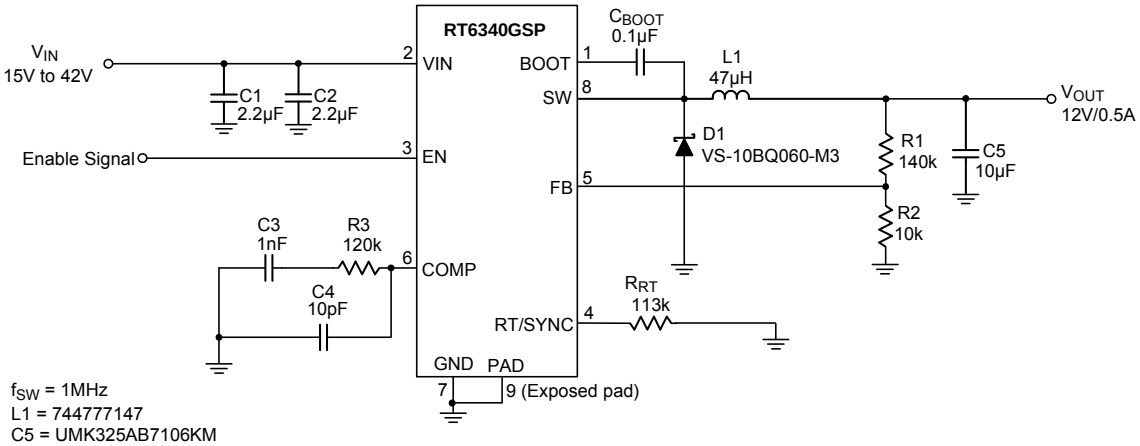
f_{SW} = 300kHz
L1 = 7447713680
C5 = GRM32ER61C476KE15L
C1/C2 = HMK316AC7225KL-TE

500kHz, 5V, 0.5A Step-Down Converter



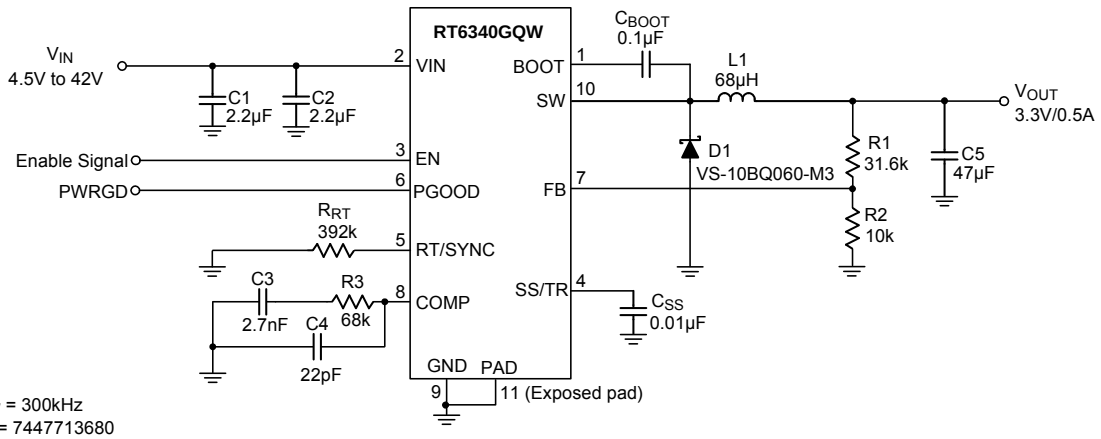
f_{SW} = 500kHz
L1 = 744777147
C5 = GRM32ER61C476KE15L
C1/C2 = HMK316AC7225KL-TE

1MHz, 12V, 0.5A Step-Down Converter



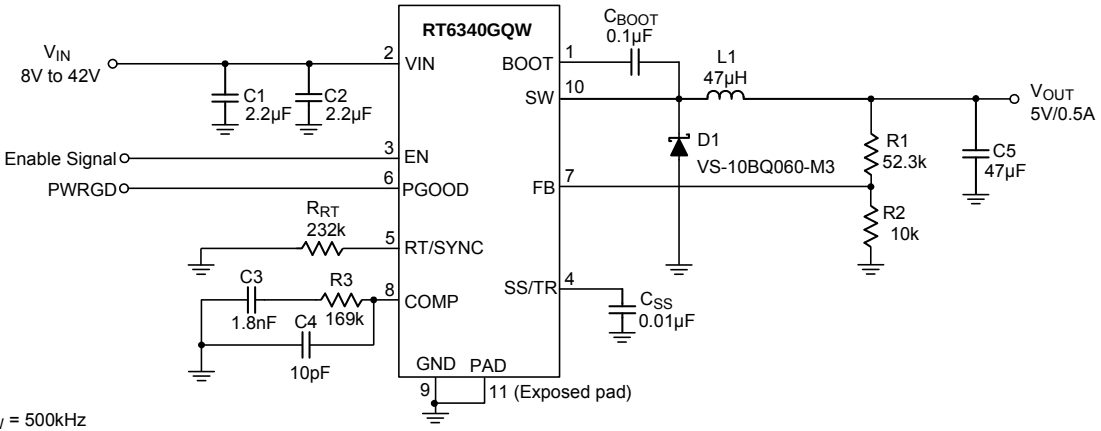
f_{SW} = 1MHz
L1 = 744777147
C5 = UMK325AB7106KM
C1/C2 = HMK316AC7225KL-TE

300kHz, 3.3V, 0.5A Step-Down Converter



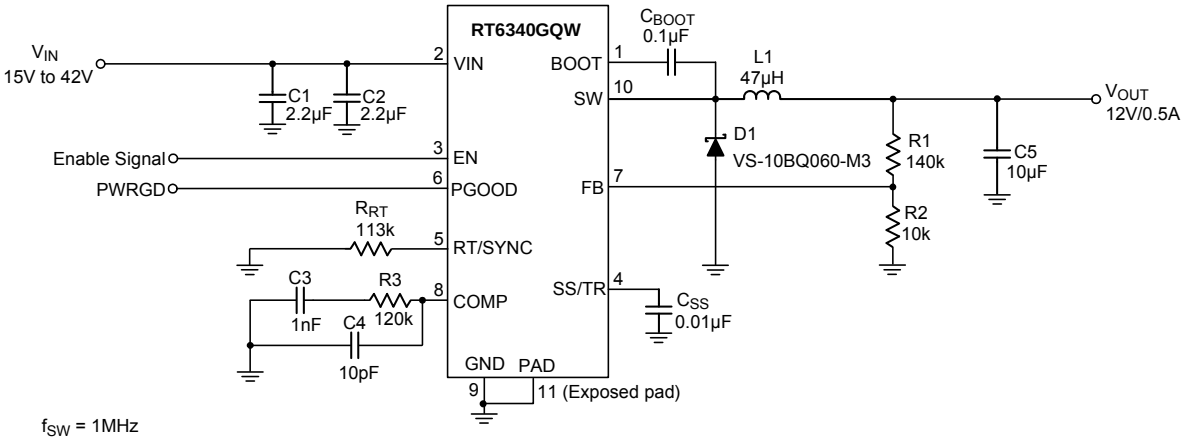
f_{SW} = 300kHz
L1 = 7447713680
C5 = GRM32ER61C476KE15L
C1/C2 = HMK316AC7225KL-TE

500kHz, 5V, 0.5A Step-Down Converter



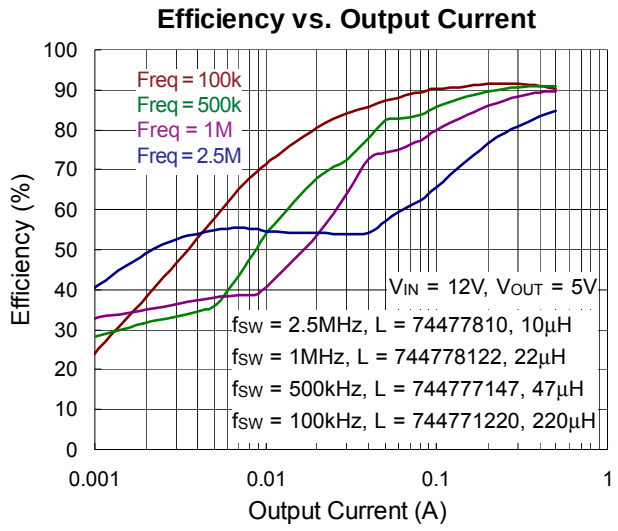
f_{SW} = 500kHz
L1 = 744777147
C5 = GRM32ER61C476KE15L
C1/C2 = HMK316AC7225KL-TE

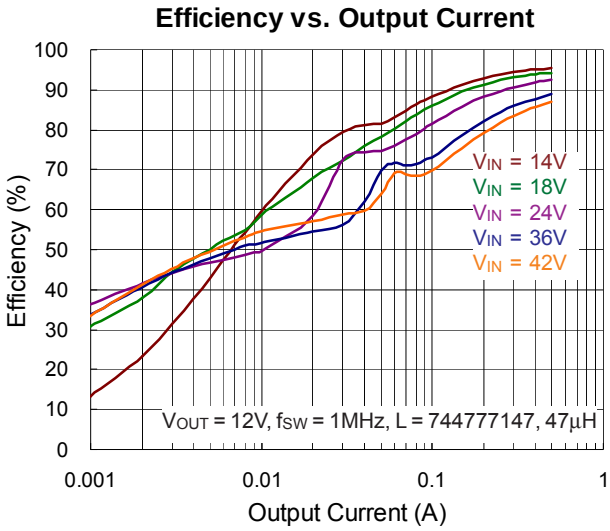
1MHz, 12V, 0.5A Step-Down Converter

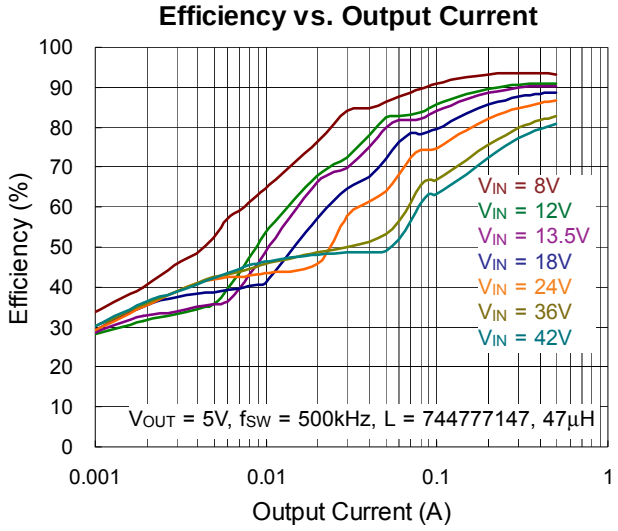


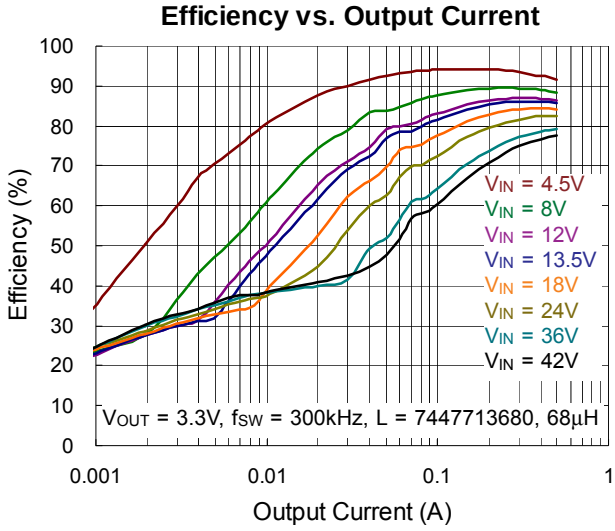
f_{SW} = 1MHz
L1 = 744777147
C5 = UMK325AB7106KM
C1/C2 = HMK316AC7225KL-TE

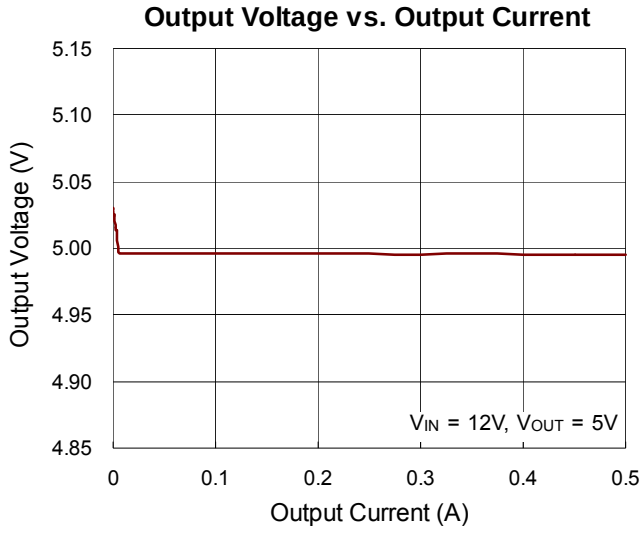
Typical Operating Characteristics

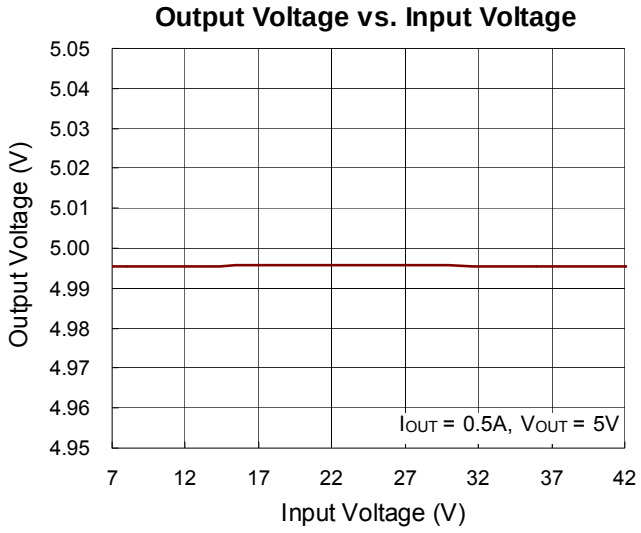




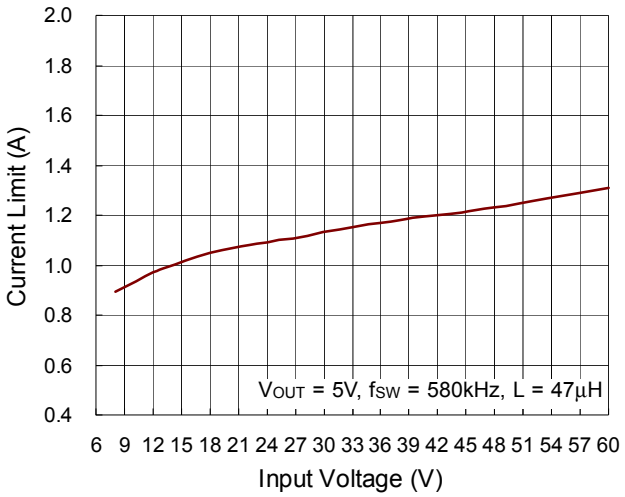




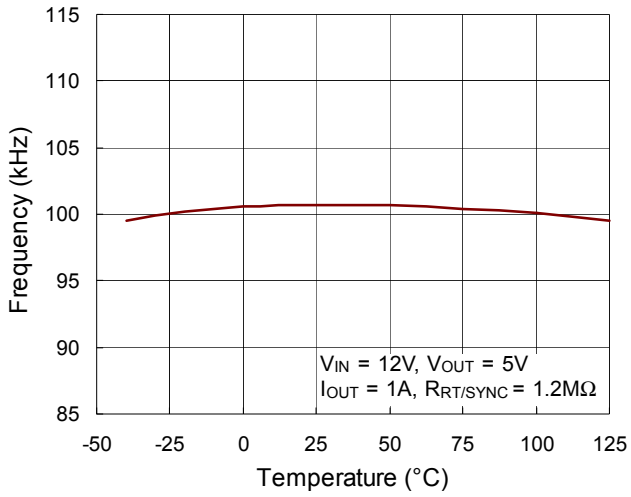




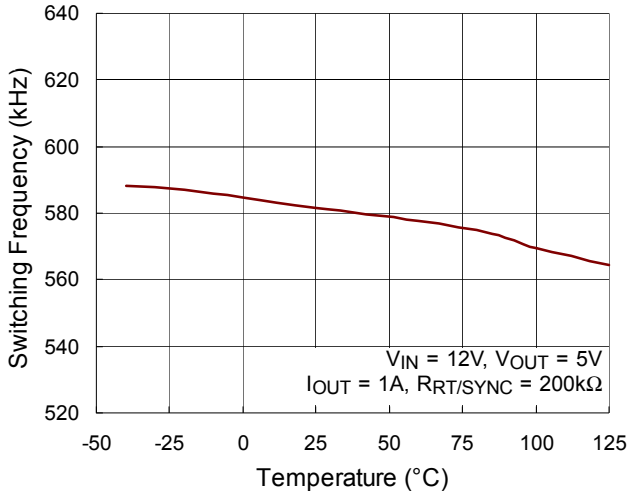
Current Limit vs. Input Voltage



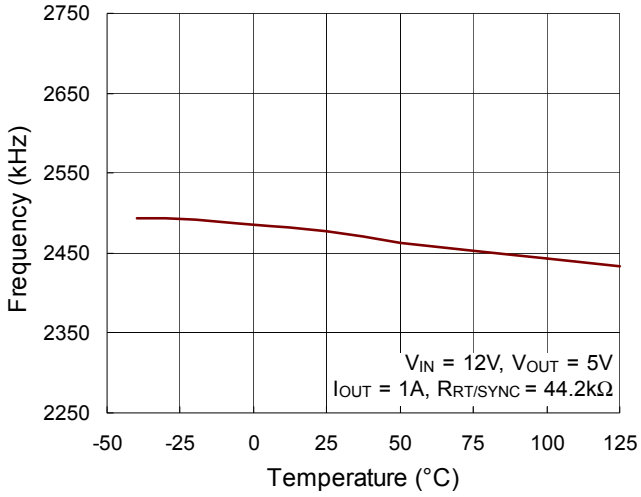
Switching Frequency vs. Temperature



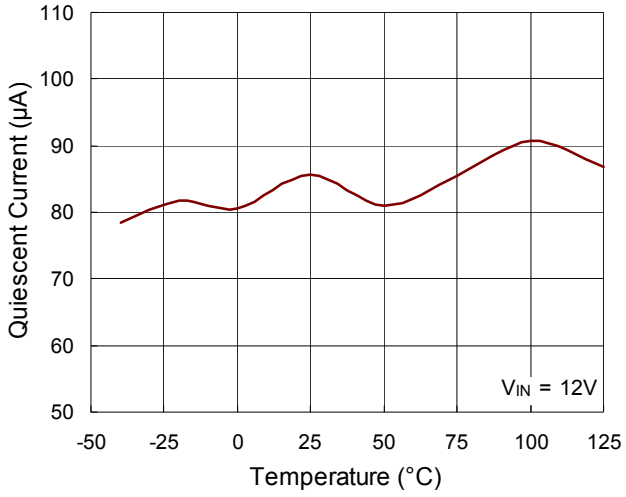
Switching Frequency vs. Temperature



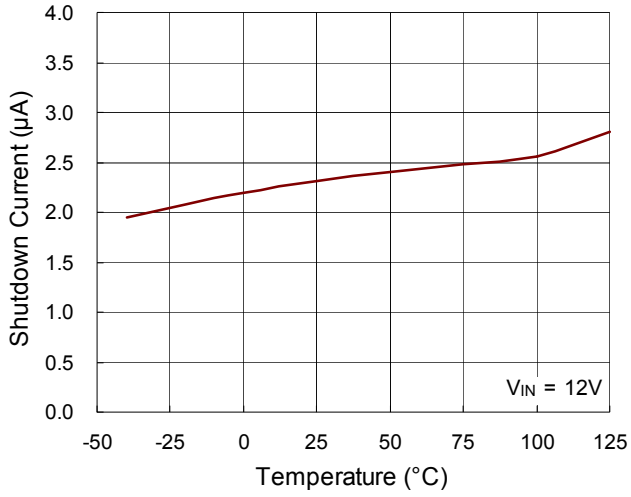
Switching Frequency vs. Temperature



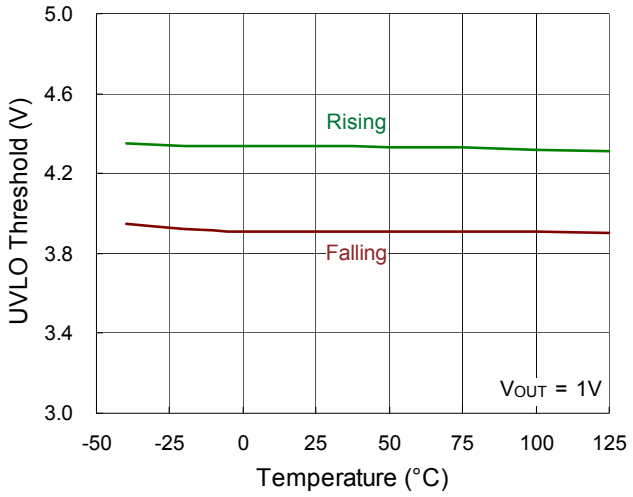
Quiescent Current vs. Temperature



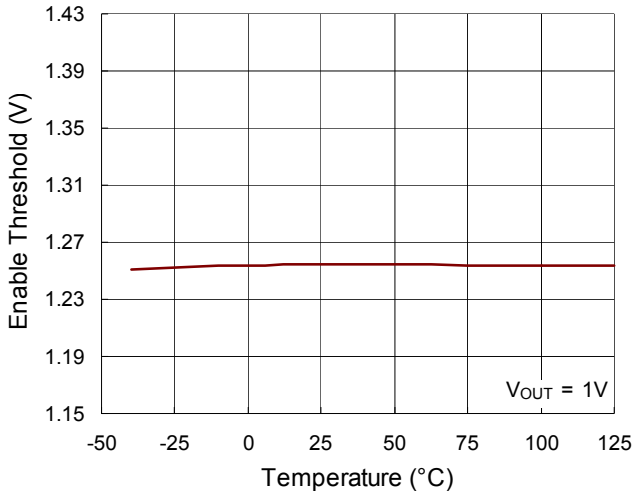
Shutdown Current vs. Temperature



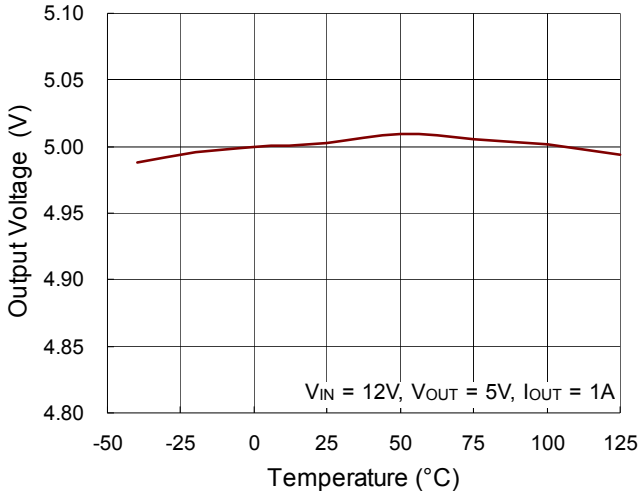
UVLO Threshold vs. Temperature



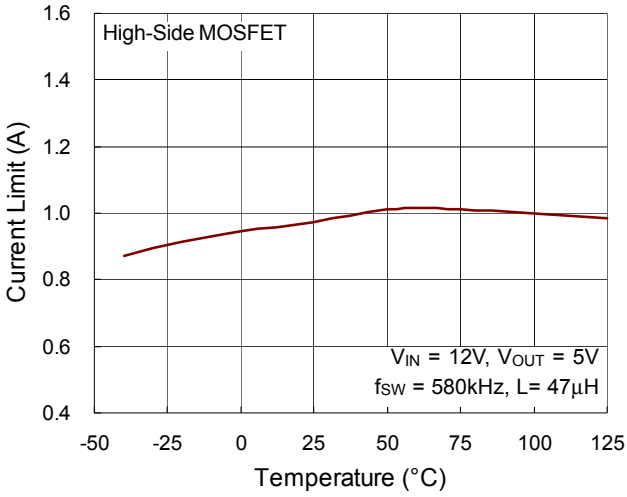
Enable Threshold vs. Temperature



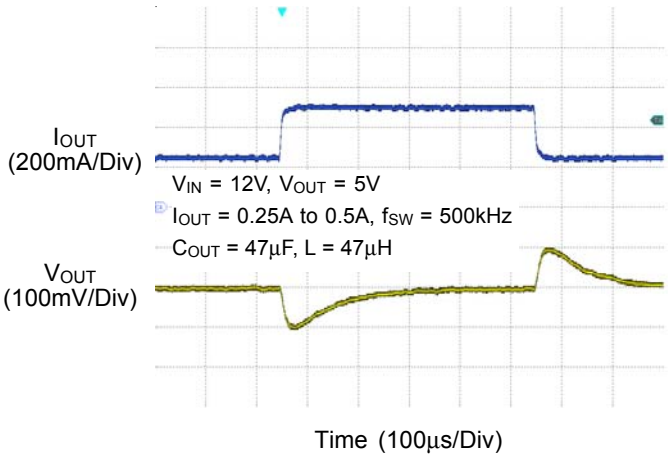
Output Voltage vs. Temperature



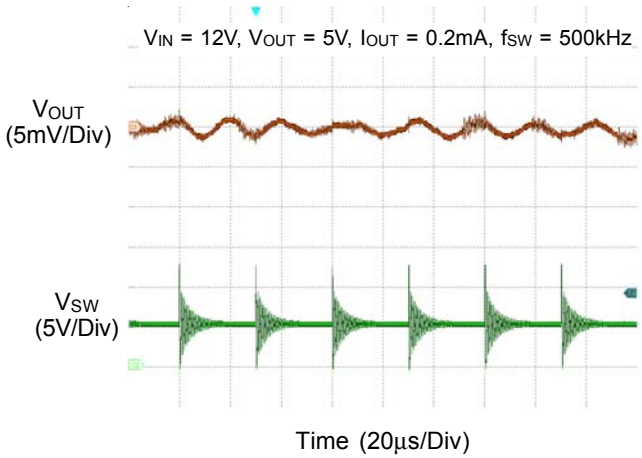
Current Limit vs. Temperature



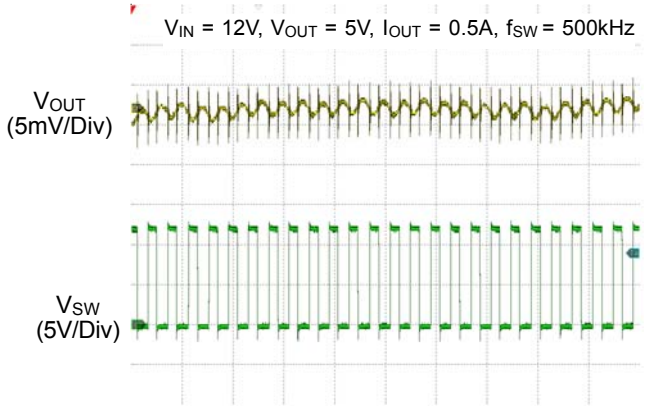
Load Transient Response



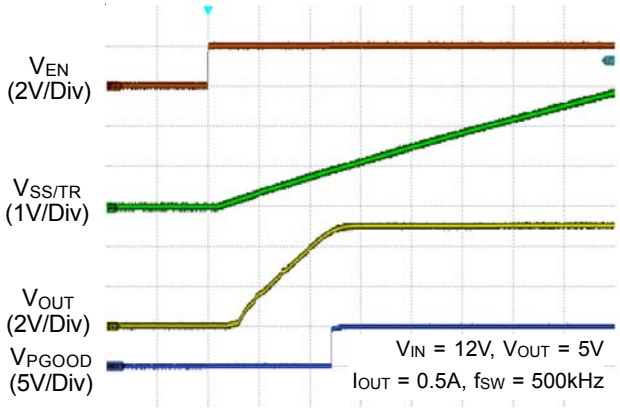
Output Ripple Voltage



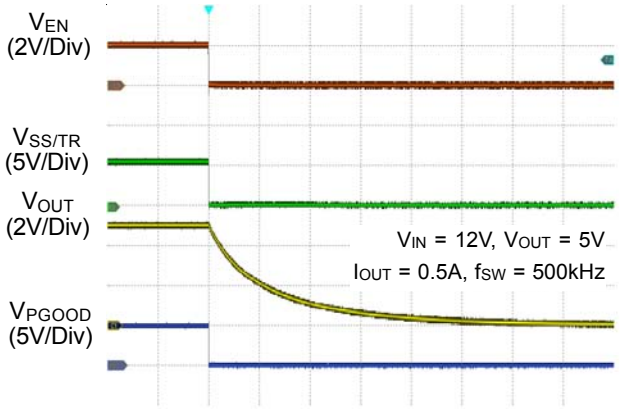
Output Ripple Voltage



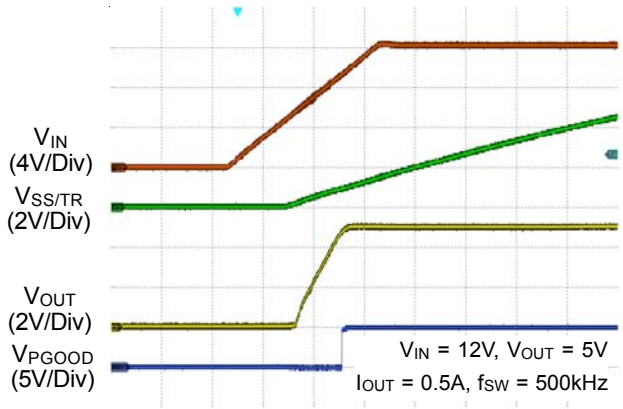
Power On from EN



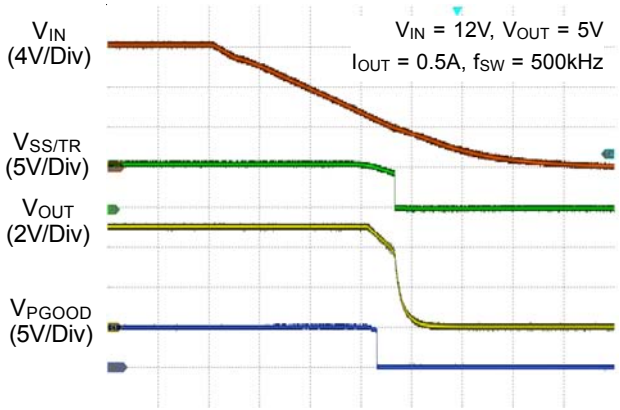
Power Off from EN



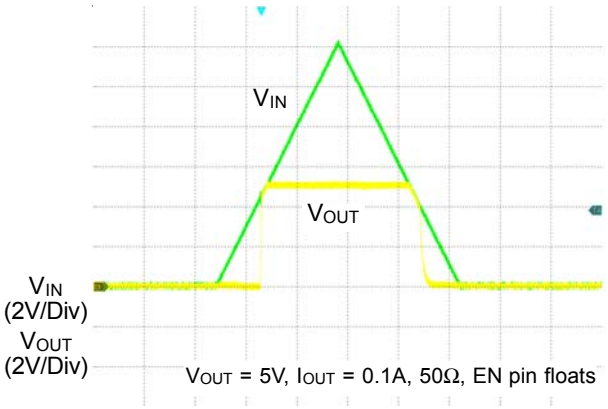
Power On from VIN



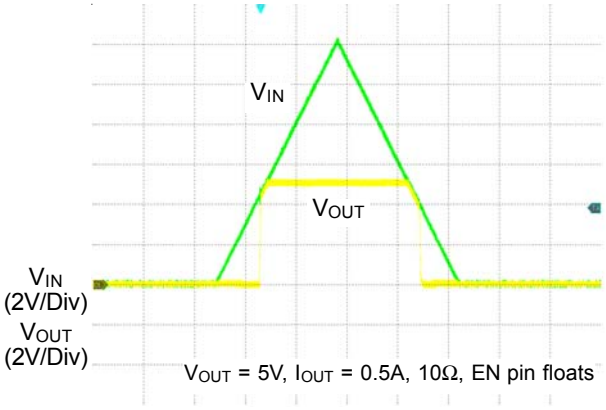
Power Off from VIN



Start-Up Dropout Performance



Start-Up Dropout Performance



Application Information

A general RT6340 application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the switching frequency selection by using external resistor $R_{RT/SYNC}$. Next, the inductor L, the input capacitor C_{IN}, the output capacitor C_{OUT} and freewheel diode are chosen. Next, feedback resistors and compensation circuit are selected to set the desired output voltage and crossover frequency, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN, external soft-start, PGOOD, and synchronization.

Switching Frequency Setting

The RT6340 offers adjustable switching frequency setting and the switching frequency can be set by using external resistor $R_{RT/SYNC}$. The switching frequency range is from 100kHz to 2.5MHz. The selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The additional constraints on operating frequency are the minimum on-time and minimum off-time. The minimum on-time, t_{ON_MIN}, is the smallest duration of time in which the high-side switch can be in its "on" state. The minimum on-time of the RT6340 is 100ns (typically). In continuous mode operation, the maximum operating frequency, f_{SW_MAX}, of can be derived from the minimum on-time according to the formula below :

$$f_{SW\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times V_{IN\_MAX}}$$

where V_{IN_MAX} is the maximum operating input voltage.

The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RT6340 is capable of tripping the current comparator and turning the high-side MOSFET back off. The minimum off-time of the RT6340 is 130ns (typically). If the switching frequency should be constant, the required off-time needs to be larger than minimum off-time. Below shows minimum off-time calculation with loss terms consideration :

$$t_{OFF\_MIN} \leq \frac{1 - \left[\frac{V_{OUT} + \left(I_{OUT\_MAX} \times R_L\right) + V_D}{V_{IN\_MIN} - \left(I_{OUT\_MAX} \times R_{DS(ON)\_H}\right) - V_D} \right]}{f_{SW}}$$

where $R_{DS(ON)\_H}$ is the on-resistance of the high-side MOSFET; V_D is the forward conduction voltage of the freewheel diode; R_L is the DC resistance of inductor.

The switching frequency f_{SW} is set by the external resistor $R_{RT/SYNC}$ connected between the RT/SYNC pin and ground. The failure mode and effects analysis (FMEA) consideration is applied to the RT/SYNC pin setting to avoid abnormal switching frequency operation at failure conditions. It includes failure scenarios of short-circuit to ground and the pin is left open. The switching frequency will be 900kHz (typically) when the RT/SYNC pin is shorted to ground, and 240kHz (typically) when the pin is left open. The equation below shows the relation between setting frequency and the $R_{RT/SYNC}$ value.

$$R_{RT/SYNC\ (k\Omega)} = \frac{140398}{f_{SW}^{1.03}}$$

where f_{SW} (kHz) is the desired setting frequency. It is recommended to use 1% tolerance or better, and the temperature coefficient of 100 ppm or less resistors. Figure 4 shows the relationship between switching frequency and the $R_{RT/SYNC}$ resistor.

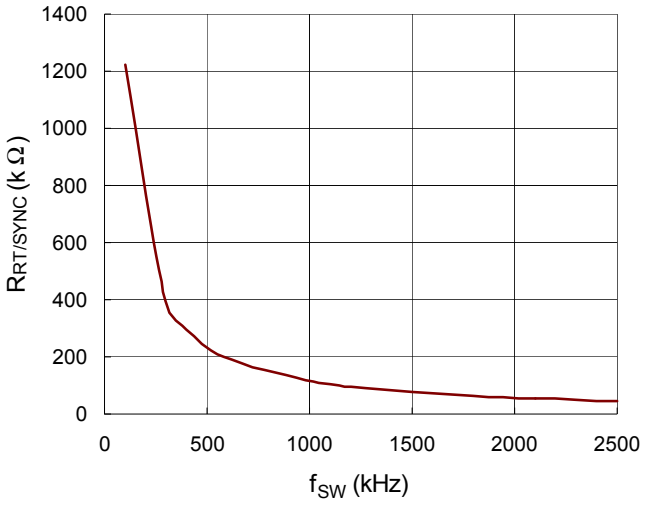


Figure 4. Switching Frequency vs. $R_{RT/SYNC}$

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This results in additional phase lag in the loop and reduces the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold and increases the AC losses in the inductor. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%. When duty cycle exceeds 50%, below condition needs to be satisfied :

$$0.5 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (0.5A).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above . In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating which is equal to or greater than the switch current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET. The C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 5 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors.

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} is maximum input ripple voltage.

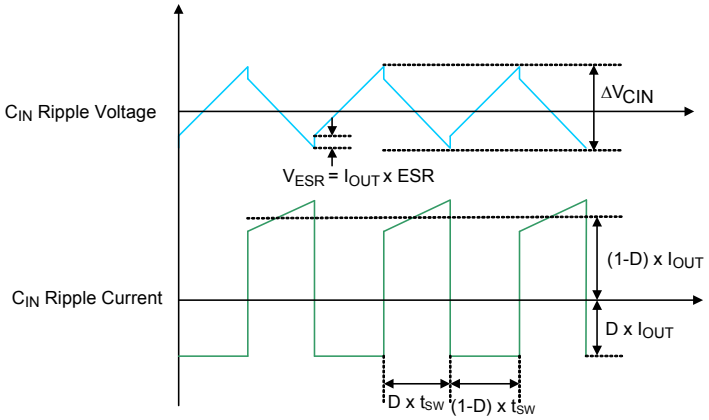


Figure 5. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of its small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT6340 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin with a low inductance connection to the GND of the IC. The VIN pin must be bypassed to ground with a minimum value of effective capacitance 1.5μF. For 500kHz switching frequency application, two 2.2μF, X7R capacitors can be connected between the VIN pin and the GND pin. The larger input capacitance is required when a lower switching frequency is used. For filtering high frequency noise, an additional small 0.1μF capacitor should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

Where the ΔI_L is the peak-to-peak inductor ripple current. The output highest ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, and can be calculated from below equation :

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The X7R dielectric capacitor is recommended for the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated values when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

Freewheel Diode Selection

When the high-side MOSFET turns off, inductor current

is supplied through the external low-side diode, freewheel diode, connected between the SW pin and GND.

The reverse voltage rating of freewheel diode should be equal to or greater than the V_{IN_MAX}. The maximum average forward rectified current of freewheel diode should be equal to or greater than the maximum load current. Considering the efficiency performance, the diode must have a minimum forward voltage and reverse recovery time. So Schottky Diodes are recommended to be freewheel diode.

The select forward voltage of Schottky Diode must be less than the restriction of forward voltage in Figure 6 at operating temperature range to avoid the IC malfunction.

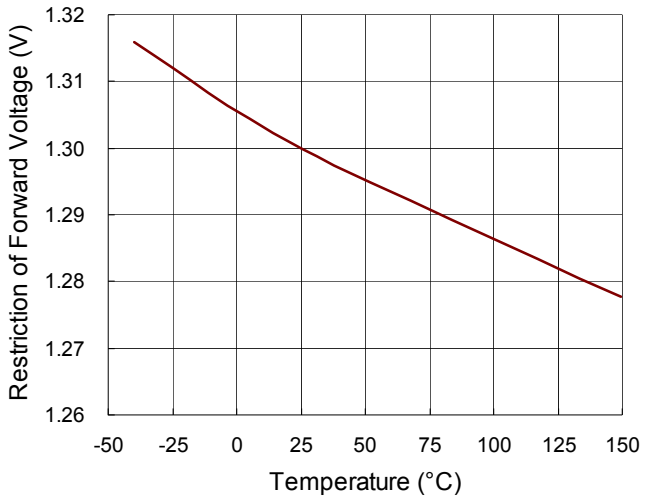


Figure 6. Restriction of Forward Voltage vs. Temperature

The losses of freewheel diode must be considered in order to ensure sufficient power rating for diode selection. The conduction loss in the diode is determined by the forward voltage of the diode, and the switching loss in the diode can be determined by the junction capacitor of the diode. The power dissipation of the diode can be calculated as following formula

$$P_D = P_{D\_CON} + P_{D\_SW} = I_{OUT} \times V_D \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$+ \frac{1}{2} \times C_J \times (V_{IN} + V_D)^2 \times f_{SW}$$

where C_J is the junction capacitance of the freewheel diode.

Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 7. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage V_{REF}, is 0.8V (typically).

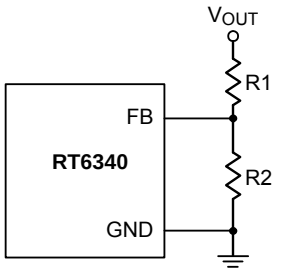


Figure 7. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 should not be larger than 80kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operation. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFET and so on.

In most cases, the peak current mode control architecture used in the RT6340 only requires two external components to achieve a stable design as shown in Figure 8. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. At around the crossover frequency, the peak current mode control (PCMC) equivalent circuit of Buck converter can be simplified as shown in Figure 9. The method presented here is easy to calculate and ignore the effects of the internal slope compensation. Since the slope

compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of the circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the steps below to calculate the compensation components :

1. Set up the crossover frequency, f_C. For stability purposes, the target is to have a loop gain slope that is −20dB/decade from a very low frequency to beyond the crossover frequency. In general, one-twentieth to one-tenth of the switching frequency (5% to 10% of fsw) is recommended to be the crossover frequency. Do "NOT" design the crossover frequency over 80kHz with the RT6340. For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside of the high bandwidth is that it increases the susceptibility of the regulators to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

2. R_{COMP} can be determined by :

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF} \times gm\_cs} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_cs} \times \frac{R1 + R2}{R2}$$

where gm is the error amplifier gain of trans-conductance (97μA/V); gm_cs is COMP to current sense trans-conductance (2A/V); the variation of C_{OUT} with temperature, DC bias voltage and switching frequency needs to be taken into consideration.

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading (R_L). Calculate C_{COMP}:

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4. The compensation pole is set to the frequency at the ESR zero or 1/2 of the operating frequency. Output capacitor and its ESR provide a zero, and optional C_{COMP2} can be used to cancel this zero.

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2 \times \pi \times \frac{fsw}{2} \times R_{COMP}}$$

Note: Generally, C_{COMP2} is an optional component used to enhance noise immunity.

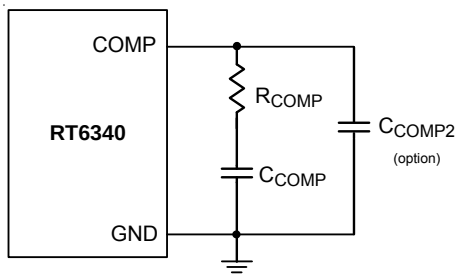


Figure 8. External Compensation Components

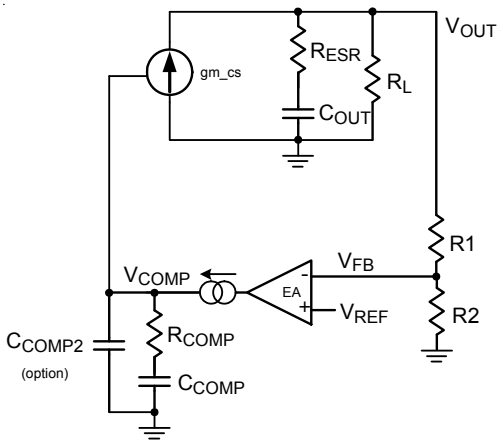


Figure 9. Simplified Equivalent Circuit of Buck with PCMC

Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the bootstrap capacitor is charged through an internal diode to an internal voltage source each time when the low-side freewheel diode conducts. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1μF, 0603

ceramic capacitor with X7R is recommended, and the capacitor should have a 6.3 V or higher voltage rating.

External Bootstrap Diode

It has to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the high-side MOSFET and improve efficiency when the input voltage is below 5.5V or duty ratio is higher than 65%. The recommended application circuit is shown in Figure 10. The bootstrap diode can be a low-cost one, such as 1N4148. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6340. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. Figure 11 shows efficiency comparison between with and without bootstrap diode.

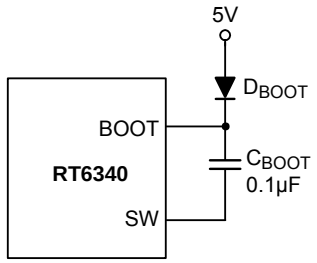


Figure 10. External Bootstrap Diode

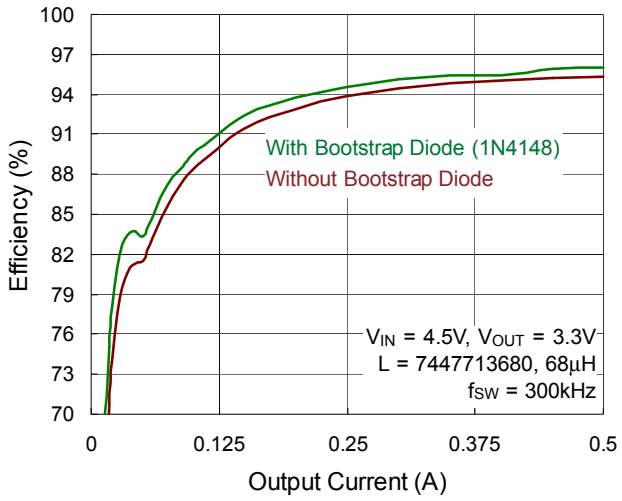


Figure 11. Efficiency Comparison between with and without Bootstrap Diode

External Bootstrap Resistor (Option)

The gate driver of an internal high-side MOSFET, utilized as a high-side switch, is optimized for turning on the switch. The gate driver is not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side MOSFET is be turned off, the SW node will be discharged relatively slow by the inductor current because the presence of the dead time when both the high-side MOSFET and low-side freewheel diode are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side MOSFET can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor as shown in Figure 12. The recommended range for the R_{BOOT} is several ohms to 10 ohms, and it could be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal high-side MOSFET, the recommended application circuit is shown in Figure 13, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection.

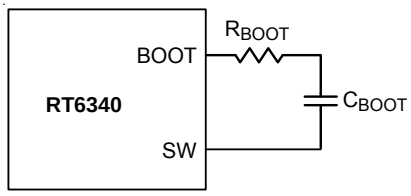


Figure 12. External Bootstrap Resistor at the BOOT Pin

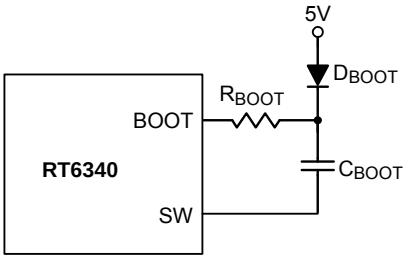


Figure 13. External Bootstrap Diode and Resistor at the BOOT Pin

EN Pin for Start-Up and UVLO Adjustment

For automatic start-up, the EN pin has an internal pull-up current source I_{EN} (0.9μA, typically) that enables operation of the RT6340 when the EN pin floats. If the EN voltage rises above the V_{TH_EN} (1.25V, typically) and the VIN voltage is higher than V_{UVLOH} (4.3V, typically), the device will be turned on, that is, switching is enabled and soft-start sequence is initiated. If the high UVLO is required, the EN pin can be used to adjust the under-voltage lockout (UVLO) threshold and hysteresis. There is an additional hysteresis current source I_{EN_Hys} (2.9μA, typically) which is sourced out of the EN pin when the EN pin voltage exceeds V_{TH_EN}. When the EN pin drops below V_{TH_EN}, the I_{EN_Hys} is removed. Therefore, the EN pin can be externally connected to V_{IN} by adding two resistors, R_{ENH} and R_{ENL} to achieve UVLO adjustment as shown in Figure 14.

According to the desired start and stop input voltage, the resistance of R_{EN1} and R_{EN2} can be obtained as below :

$$R_{EN1} = \frac{V_{Start} - V_{Stop}}{I_{EN\_Hys}}$$

$$R_{EN2} = \frac{V_{TH\_EN}}{\frac{V_{Start} - V_{TH\_EN}}{R_{EN1}} + I_{EN}}$$

The EN pin, with high-voltage rating, supports wide input voltage range to adjust the VIN UVLO.

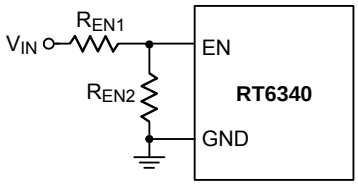


Figure 14. Resistive Divider for Under-Voltage Lockout Threshold Setting

Soft-Start and Tracking Control

The RT6340GQW provides adjustable soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. The RT6340GQW provides an SS/TR pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor $C_{SS/TR}$ connected from the SS/TR pin to ground or controlled by external ramp voltage to SS/TR pin. An internal current source I_{SS} (2μA, typically) charges an external capacitor to build a soft-start ramp voltage. The internal charging current source I_{SS} gradually increases the voltage on $C_{SS/TR}$, and the high-side MOSFET will start switching if voltage difference between SS/TR pin and FB pin is equal to 75mV (i.e. $V_{SS/TR} - V_{FB}$ = 75mV, typically) during power-up period. The FB voltage will track the SS/TR pin ramp voltage with a SS/TR to FB offset voltage (75mV, typically) during soft-start interval. The typical soft-start time (t_{SS}) which is the duration of V_{OUT} rises from 10% to 90% of setting value is calculated as follows :

$$t_{SS} = C_{SS/TR} \times \frac{V_{REF} \times 0.8}{I_{SS}}$$

If a heavy load is added to the output with large capacitance, the output voltage will never enter regulation because of UVP. Thus, the device remains in hiccup operation. The $C_{SS/TR}$ should be large enough to ensure soft-start period ends after C_{OUT} is fully charged.

$$C_{SS/TR} \geq C_{OUT} \times \frac{I_{SS} \times V_{OUT}}{0.8 \times I_{COUT\_CHG}}$$

where I_{COUT_CHG} is the C_{OUT} charge current which is related to the switching frequency, inductance, high-side MOSFET peak current limit and load current.

Power-Good Output

The RT6340GQW features an open-drain power-good output (PGOOD) to monitor the output voltage status. The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

It is recommended to use pull-up resistance between the values of 1 and 10kΩ to reduce the switching noise coupling to PGOOD pin.

Synchronization

The RT6340 can be synchronized with an external clock ranging from 300kHz to 2.2MHz which is applied to the RT/SYNC pin. The minimum synchronous pulse width of the external clock applied to the RT/SYNC pin must be larger than 40ns and the amplitude should have valleys that are below 0.5V and peaks above 2.2V (up to 6V). The rising edge of the SW will be synchronized to the falling edge of the RT/SYNC pin signal.

The switching frequency control of the RT6340 will switch from the RT resistor setting mode to the synchronization mode when the external clock is applied to the RT/SYNC pin. The RT6340 transitions from the RT resistor setting mode to the synchronization mode within 60 microseconds. Figure 15 and Figure 16 show the device synchronized to an external system clock in power saving mode (PSM) and continuous conduction mode (CCM).

The sub-harmonic oscillation may occur for duty cycle greater than 50% in CCM at synchronization mode. By choosing a larger inductor, more slope compensation can be achieved and the risk of such sub-harmonic oscillations is eliminated.

The switching frequency of synchronization should be equal to or higher than the frequency set with the RT resistor. For example, if the switching frequency of synchronization will be 500kHz and higher, the $R_{RT/SYNC}$ should be selected for 500kHz. Be careful to design the compensation network and inductance for switching frequency controlled by both RT resistor setting mode and the synchronization mode.

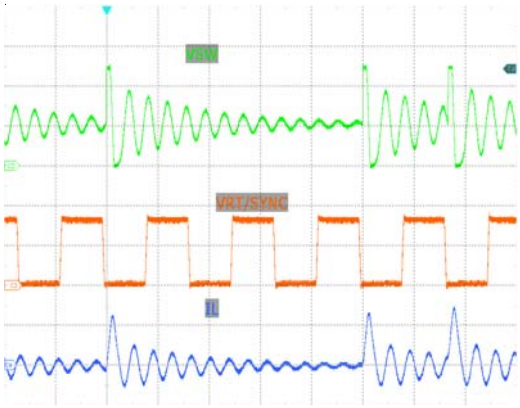


Figure 15. Synchronization Mode in PSM

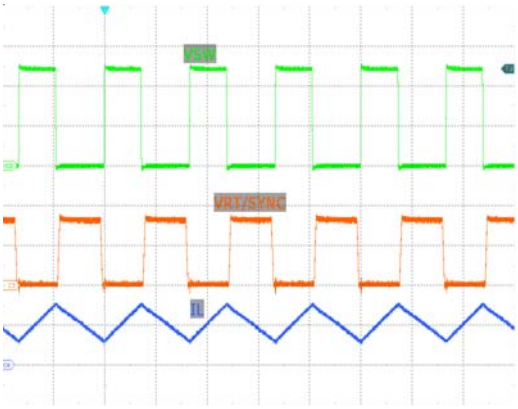


Figure 16. Synchronization Mode in CCM

Thermal Considerations

In many applications, the RT6340 does not generate much heat due to its high efficiency and low thermal resistance of its WDFN-10SL 3x3 and SOP-8 (Exposed pad) packages. However, in applications which the RT6340 runs at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RT6340 stops switching the high-side MOSFET until the temperature cools down by 15°C.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$$

where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance. Carefully select the freewheel diode to ensure

that thermal performance will not be limited by the freewheel diode.

If the application calls for a higher ambient temperature and may exceed the recommended maximum junction temperature of 150°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RT6340 :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN3} as close to the IC as possible to reduce the loop impedance and minimize switch node ringing.
- Place bootstrap capacitor, C_{BOOT}, as close to the IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and GND, and close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible. Add thermal vias under and near the RT6340 to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Place freewheel diode, D1, and inductor, L1, as close to the IC as possible to reduce the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components R_{FB1} / R_{FB2} near the IC.
- Place the compensation components R_{CP1} / C_{CP1} / C_{CP2} near the IC.
- The RT/SYNC resistor, $R_{RT/SYNC}$, should be placed as close to the IC as possible because to the RT/SYNC pin is sensitive to noise.

Figure 17 and Figure 18 are the RT6340GQW layout examples.

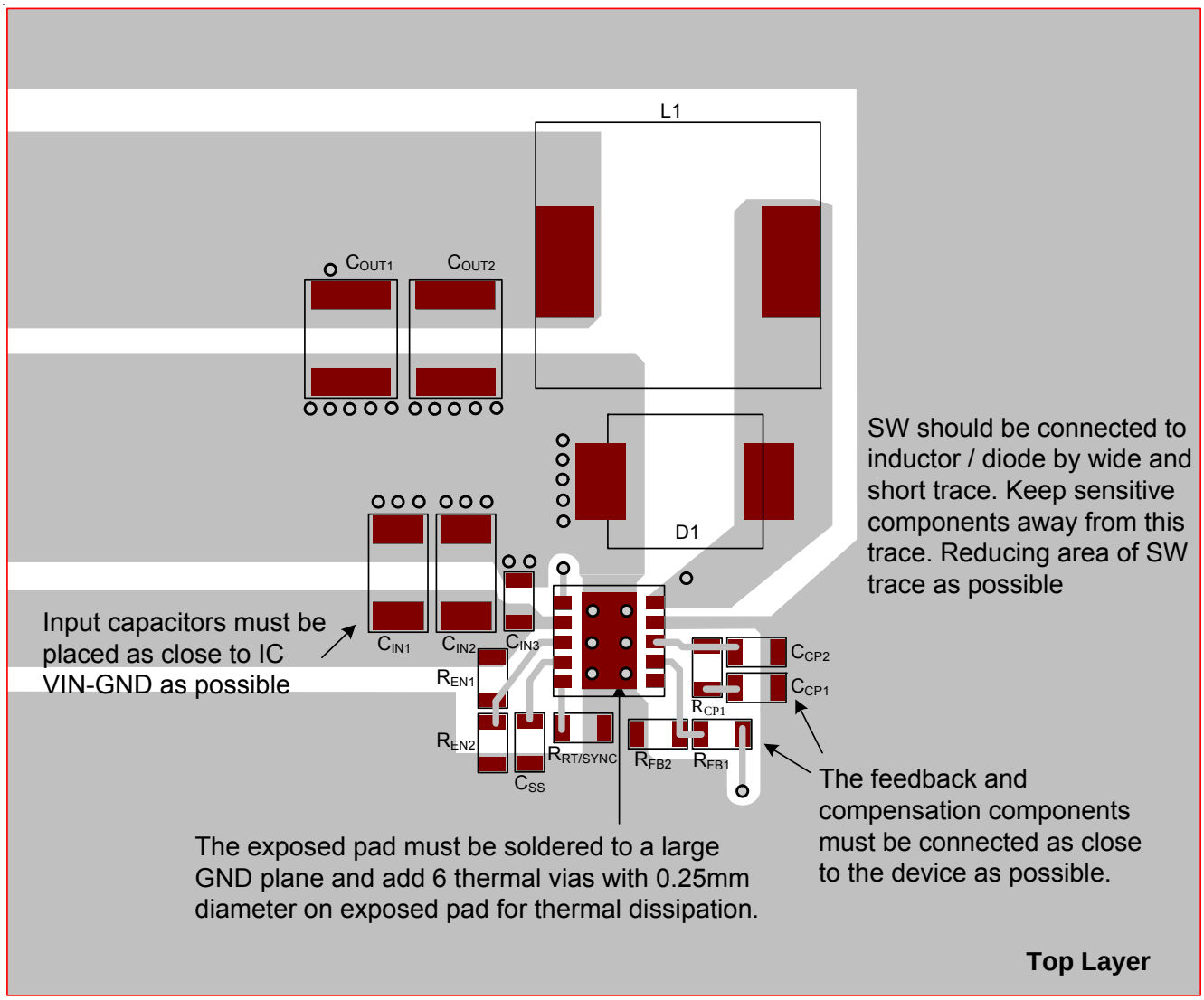


Figure 17. Layout Guide for RT6340GQW (Top Layer)

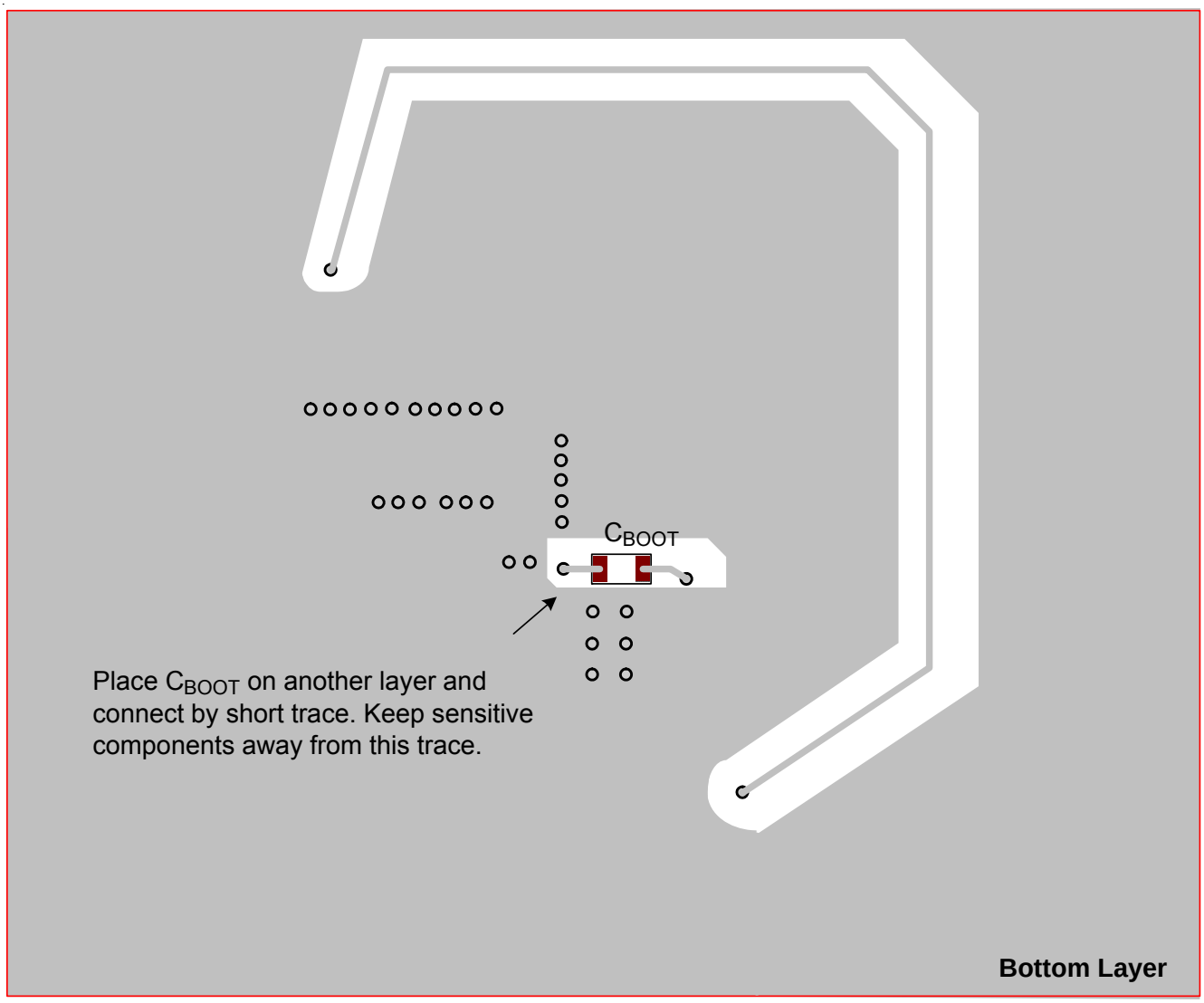
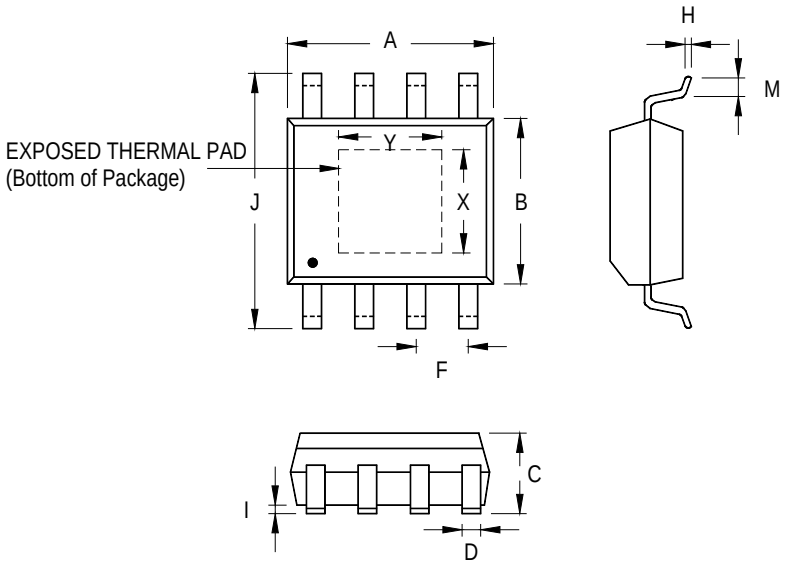


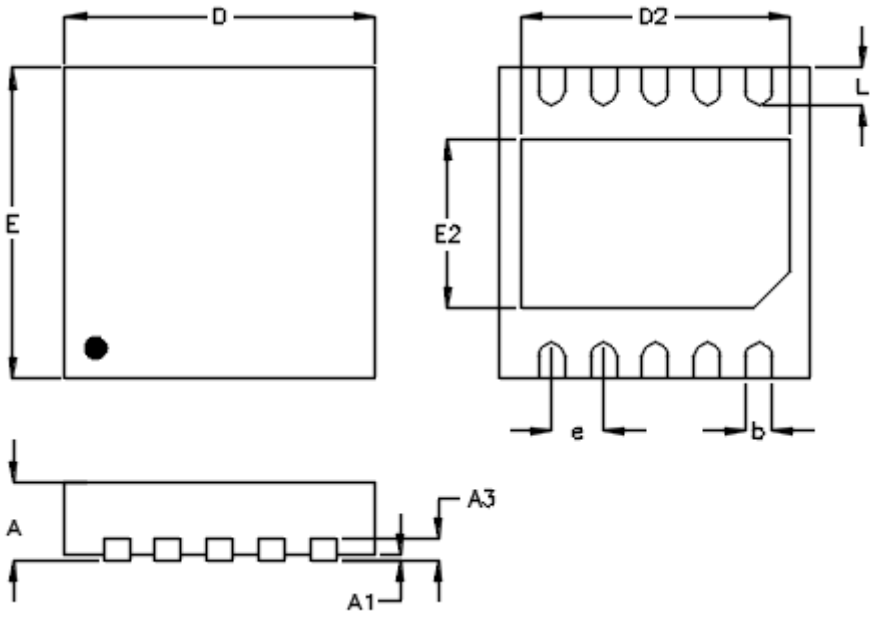
Figure 18. Layout Guide for RT6340GQW (Bottom Layer)

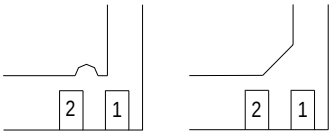
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

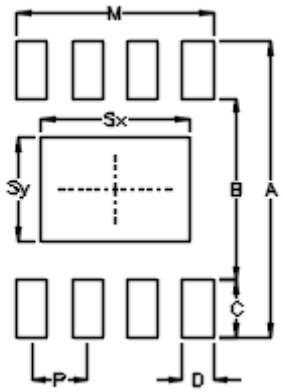
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

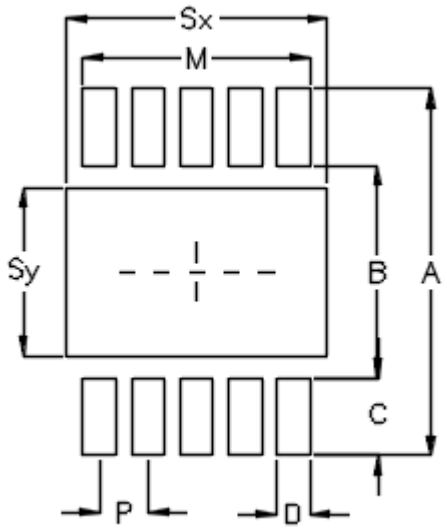
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.550	2.650	0.100	0.104
E	2.900	3.100	0.114	0.122
E2	1.590	1.690	0.063	0.067
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 10SL DFN 3x3 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3*3-10S	10	0.50	3.80	2.20	0.80	0.35	2.70	1.74	2.35	±0.05

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